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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/067,845	02/08/2002	Yun-Bok Lee	8733.592.00	9648

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MCKENNA LONG & ALDRIDGE LLP
1900 K STREET, NW
WASHINGTON, DC 20006

EXAMINER	
CHOWDHURY, TARIFUR RASHID	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 03/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/067,845	LEE, YUN-BOK	
	Examiner	Art Unit	
	Tarifur R Chowdhury	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *1-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 12-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (AAPA) in view of Tanaka, USPAT 5,990,987.

3. The AAPA described (pages 5-9) and shown in Figs 4A-4G, 5A-5G and 6A-6G, a method of forming an array substrate for in-plane switching type liquid crystal display device, the method comprising:

- forming a first metal layer on a substrate;
- patterning the first metal layer using a mask to form a gate line having a gate electrode and a common line having a plurality of common electrodes (page 6, paragraph 0014);
- forming a gate insulating layer (82) on the substrate (1) to cover the patterned first metal layer (page 7, paragraph 0017);
- forming a semiconductor layer (84a) on the gate insulating layer using a mask;
- forming a second metal layer on the gate insulating layer to cover the semiconductor layer;

- patterning the second metal layer using a mask to form a data line having a source electrode, a pixel connecting line connecting a plurality of pixel electrodes, and a drain electrode that is spaced apart from the source electrode (page 7,paragraph 0019);
- forming a channel by etching a portion of an semiconductor layer (84a) between the source and drain electrodes (page 7, paragraph 0020);
- forming an alignment layer over the substrate to cover the patterned second metal layer (page 9, paragraph 0026); and
- thermal-treating the substrate having the alignment layer and the source and drain electrode (page 9, paragraph 0028);

The only difference between the method described in the AAPA and the instant invention is that in the AAPA about four masks are used in the method of the AAPA compared to three masks used in the instant invention.

Tanaka discloses a method of forming an array substrate for an in-plane switching type liquid crystal display wherein a first mask is used to form data line having a source electrode, a pixel connecting line connecting a plurality of pixel electrodes, and a drain electrode, a second mask to form semiconductor layer and a third mask to form a gate line having a gate electrode and a common line having a plurality of common electrodes (abstract). Tanaka also discloses that by using reduced photolithographic steps (less masks) to produce an array substrate for a liquid crystal display is advantageous since it reduces cost and improve production yield (col. 2,lines 51-67).

Tanaka is evidence that ordinary workers in the art would find a reason,

suggestion or motivation to use less masks to form an array substrate for a liquid crystal display.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the method of manufacturing the array substrate for an in-plane switching type liquid crystal display described in the AAPA by adopting a method wherein less photolithographic steps are used to form the elements as in the instant invention so that production yield is improved and thus cost is reduced, as per the teachings of Tanaka.

Further, as to the limitation of simultaneously thermal-treating the alignment layer, the source electrode and the drain electrode, it is a very well known practice in the art to reduce manufacturing steps and thus cost and therefore it would have at least been obvious to one of ordinary skill in the art at the time of the invention was made to simultaneously thermal-treating the alignment layer, the source electrode and the drain electrode to reduce manufacturing steps and thus cost.

Accordingly, claims 12, 20-23 would have been obvious.

As to claims 13 and 14, performing the thermal treatment at a temperature of 200 to 230 degrees centigrade for 3 to 4 hours is common and known in the art and thus would have been obvious to avail a proven technique.

As to claims 15-19, the AAPA described in the present application also discloses that the alignment layer is cured during the thermal treatment and the step of annealing the thin film transistor that includes the source electrode and drain electrodes, the gate

electrode and the semiconductor layer and that the curing and annealing are contemporaneous. (page 9, paragraph 0028).

As to claim 24, the AAPA described in the present application also discloses that the method further comprising rubbing the alignment layer (page 9, paragraph 0027).

As to claim 25, using a rubbing direction of 5 to 45 degrees from the common and pixel electrodes when the alignment layer is rubbed is common and known in the art and thus would have been obvious to optimize performance.

Response to Arguments

4. Applicant's arguments filed on 12/22/03 have been fully considered but they are not persuasive.

Applicant's arguments with respect to claim 12 have been considered but are moot in view of the new ground(s) of rejection.

In response to applicant's argument that the fabrication process described in Tanaka is different than the fabrication process described in the instant application, it is respectfully pointed out to applicant that both Tanaka and the instant invention discloses the formation of a source electrode, drain electrode and a pixel electrode using a mask, a semiconductor layer using another mask and a gate electrode, an active layer and a common electrode using another mask.

Further, in response to applicant's argument that Tanaka fail to teach or suggest the simultaneous thermal-treatment of the alignment layer, the source electrode and the drain electrode, it is respectfully pointed out to applicant that the admitted prior art of the instant invention discloses the step of thermal-treating the alignment layer and as to the

limitation of simultaneous treatment applicant's attention is respectfully requested the rejection above.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tarifur R Chowdhury whose telephone number is (571) 272-2287. The examiner can normally be reached on M-Th (6:30-5:00) Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TRC
March 09, 2004

TARIFUR R. CHOWDHURY
PRIMARY EXAMINER